Analysis of Crosstalk in Very High-Speed LSI/VLSI's Using a Coupled Multiconductor MIS Microstrip Line Model

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Abstract — **Crosstalk in very high-speed LSI/VLSI's is analyzed using a coupled multiconductor metal–insulator–semiconductor (MIS) microstrip line model. Loss in the substrate is ignored for simplicity. A periodic boundary condition is used, and the mode analysis is done using the Green's function method. Effects of line length, spacing, substrate thickness, and output impedance of gates are investigated. The "lumped capacitance" approximation for interconnections is shown to be inadequate for crosstalk evaluation when the circuit speed is less than 200–300 ps in LSI circuits. The result indicates that crosstalk considerations based on a transmission-line model is very important in the design of very high-speed LSI/VLSI circuits. Provisions of adjacent shield lines are shown to be significantly effective in reducing crosstalk, but at the risk of dynamic ringing and at the sacrifice of wiring capacity. A shielded multilevel interconnect scheme is proposed for reduction of crosstalk without reduction of wiring capacity.**

I. Introduction

In order to meet the increasing demands for higher speeds in areas of high-speed computation, signal processing, data links, and related instrumentation, very high-speed integrated circuits with a propagation delay time per gate t_{pd} of below 100 ps have to be developed. In SSI/MSI integration levels, t_{pd} reaching 10-ps range has already been realized with various technologies [1]–[3]. However, as one tries to achieve high speeds in LSI/VLSI levels, difficulties are anticipated to arise from increased lengths of interconnections. The purpose of this paper is to analyze the crosstalk in the interconnection system of high-speed LSI/VLSI circuits. Delay due to interconnection is analyzed in our separate paper in this issue [4].

Previous analyses on crosstalk were based either on the "lumped capacitance" approximation [5] or on the distributed-parameter models with a limited number of conductors [6]–[9]. In this paper, interconnections are modeled as a coupled multiconductor metal–insulator–semiconductor (MIS) microstrip line system having many conductors. The present model is particularly applicable to semicustom gate arrays where many closely spaced interconnections run parallel for a long distance. Loss in the semiconductor substrate is ignored for simplicity, making the model applicable to IC's formed on semi-insulating GaAs or InP substrates or silicon-on-sapphire (SOS) substrates. A periodic boundary condition is used and this greatly simplifies the analysis without too much loss generality. Mode capacitances evaluated using a Green's function method. Section II explains the model and mathematical formulation, and the result concerning crosstalk amplitude and its reduction is presented and discussed in Section III. Section IV gives the conclusion.

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II. Model and Formulation

A. Model and Boundary Condition

The MIS microstrip line model with n strip conductors is shown in Fig. 1(a). Interconnections are formed on a surface passivated semiconductor substrate with a metallized back. This model provides a good first-order approximation for closely spaced interconnection tracks in high-speed semicustom gate arrays, as shown in Fig. 2. For such a case, n corresponds to the track number or wiring capacity of the channel. Loss in the substrate is ignored, since a complicated situation due to the slow-wave mode propagation and mode transition takes place in the conducting substrate, as discussed in our separate paper [4].

As the boundary condition exists on both sides of the stripline system, a periodic boundary condition is adopted where it is assumed that the same n-conductor stripline system is repeated infinitely, as shown in Fig. 1(b). This is a convenient boundary condition for simplifying the problem, as often employed in solid-state physics. In the crosstalk problem, we are more interested in the interrelationship of strip conductors inside the wiring channel rather than effects of the channel boundaries which depend on the device and layout design. Thus, the periodic boundary condition is useful to provide a first-order estimate of crosstalk without going into the specific design details.

B. Normal Modes

Obviously, there exists n quasi-TEM normal modes on this stripline system. Let us consider an excitation in which the phase angle difference of voltage and current between two adjacent strip conductors is constant and equal to θ, and call such an elementary excitation the "θ-mode." Possible values of θ that satisfy the cyclic boundary condition are then given by

$$\theta = 0, \frac{2\pi}{n}, \cdots, \frac{2k\pi}{n}, \cdots, \frac{2(n-1)\pi}{n}. \tag{1}$$

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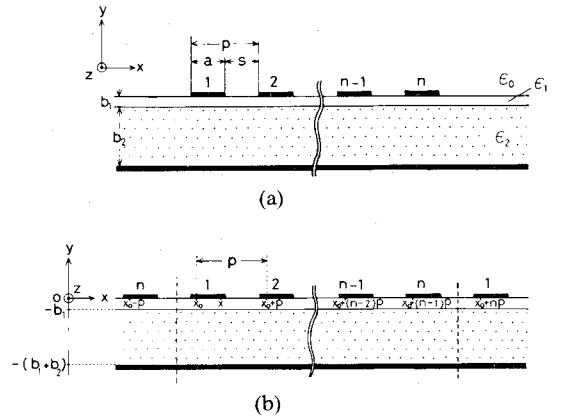


Fig. 1. (a) A coupled multiconductor MIS microstrip line model having n conductors and (b) a periodic boundary condition applied to the model.

The characteristic impedance $Z_{0\theta}$ and the phase velocity v_θ of the θ mode are given in terms of the static capacitance per conductor per unit length corresponding to the θ-mode excitation

$$Z_{0\theta} = \frac{1}{v_\theta C_\theta} \qquad v_\theta = c_0 \sqrt{\frac{C_{\theta 0}}{C_\theta}} \tag{2}$$

where $C_{\theta 0}$ is the static capacitance of the θ mode without dielectric loading, and C_θ is that with dielectric loading. c_0 is the light velocity in vacuum.

C. Line Voltage and Current

In terms of the above normal modes, the voltage and current on the kth conductor can be expressed by the following equations:

$$V_k(z) = \sum_\theta \left(A_{\theta f} e^{-j(k-1)\theta} \cdot e^{j\omega(t-(z/v_\theta))} + A_{\theta r} e^{-j(k-1)\theta} e^{j(t+(z/v_\theta))} \right) \tag{3a}$$

$$I_k(z) = \sum_\theta \left(\frac{A_{\theta f}}{Z_{0\theta}} e^{-j(k-1)\theta} e^{j\omega(t-(z/v_\theta))} - \frac{A_{\theta r}}{Z_{0\theta}} e^{-j(k-1)\theta} \cdot e^{j\omega(t+(z/v_\theta))} \right) \tag{3b}$$

where $A_{\theta f}$ is the amplitude of the θ-mode forward voltage wave and $A_{\theta r}$ is that of the backward voltage wave, z is the position on the conductor, and ω is the angular frequency. By providing terminal conditions at both ends of each conductor, mode wave amplitudes are determined. The pulse response can be obtained by a numerical inverse Laplace transform of the above equations.

D. Determination of Mode Capacitances by Green's Function Method

Values of static mode capacitances are calculated here by the Green's function method. Referring to Fig. 1(b), let $G_\theta(x, x_0)$ denote the Green's function on the strip plane ($y = 0$) for the θ-mode. It is defined as the potential at a point x on the strip plane when a unit charge with a phase factor of $\exp(-jm\theta)$ is placed at points $x_0 + mp$ with p being the pitch in Fig. 1(b) and $m = 0, \pm 1, \pm 2, \cdots, \pm\infty$. $G_\theta(x, x_0)$ can be determined by making a Fourier transformation of the two-dimensional Laplace's equation and solving the resultant equation with respect to y, as was done by Yamashita *et al.* [10]. The result is

$$G_\theta(x, x_0) = \sum_{m=-\infty}^{\infty} \frac{1}{p} \cdot e^{-j\beta_m(x-x_0)} \cdot \frac{1}{|\beta_m|} \frac{\epsilon_1 \coth|\beta_m|b_1 + \epsilon_2 \coth|\beta_m|b_2}{(\epsilon_2 \coth|\beta_m|b_2)(\epsilon_0 + \epsilon_1 \coth|\beta_m|b_1) + \epsilon_1(\epsilon_1 + \epsilon_0 \coth|\beta_m|b_1)} \tag{4}$$

where

$$\beta_m \equiv \frac{2m\pi + \theta}{p}.$$

Then, the following Fredholm integral equation of the first kind can be set up for the charge density function $\rho_\theta(x)$ for the θ-mode at point x on the strip conductor:

$$V_0 = \int_{-a/2}^{a/2} G_\theta(x, x_\theta)\rho_\theta(x_0)\, dx_0 \tag{5}$$

where V_0 is the potential on the strip under consideration. This equation can be easily solved numerically by the standard procedure [11]. Then, the static capacitance per conductor of the θ-mode can be calculated as

$$C_\theta = \frac{1}{V_0} \int_{-a/2}^{a/2} \rho_\theta(x)\, dx. \tag{6}$$

III. Results and Discussion

A. Frequency-Domain Analysis

Before going into the pulse analysis, it is desirable to check the validity of the mode analysis. To our knowledge, an analytic expression based on the conformal mapping is available for the characteristic impedance of the π-mode [12]. This analytic formula is applicable for the case of $b_1 = 0$ and $b_2 = \infty$. The values of the mode characteristic impedance calculated by the present method are compared for various a/p (a: strip width, p: pitch) ratios in Table I with those by the analytic formula. The numerical computation is done by dividing the strip into 100 segments and taking 1000 Fourier terms. As seen in Table I, the agreement between two methods is excellent with the difference being less than 0.3 percent. The calculated characteristic impedance $Z_{0\theta}$ is plotted versus a/p for various modes in

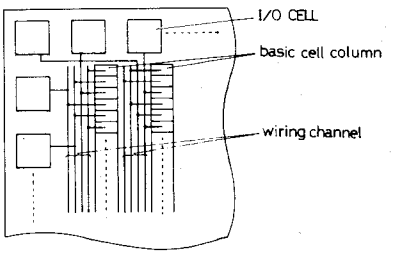


Fig. 2. A schematic diagram of a semicustom gate array.

TABLE I
COMPARISON OF CALCULATED π-MODE CHARACTERISTIC IMPEDANCE

a/p	Green's Function Method	Conformal Mapping
0.1	194.20 ohms	193.87 ohms
0.2	152.06	151.95
0.3	126.75	127.00
0.4	108.61	108.81
0.5	94.15	94.12
0.6	81.48	81.42
0.7	69.67	69.76
0.8	58.16	58.31
0.9	45.72	45.70

The values by conformal mapping are obtained by using an analytic expression in [12].

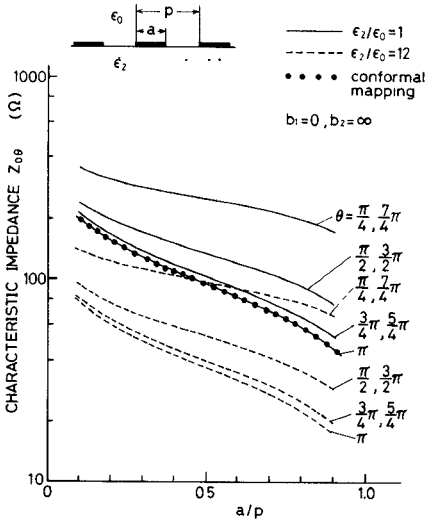


Fig. 3. Calculated characteristic impedance Z_0 of the various modes

Fig. 3. The high-impedance nature of the modes is noted; this is because of the lack of a common ground plane in this case. However, the high-impedance nature of the interconnection system remains true in the practical situation of, for instance, $a = 2$ μm, $p = 4$ μm, and $b_2 = 200$ μm, because of the small value of a/b_2.

B. Long Interconnections

The pulse response of the stripline system is calculated by the inverse Laplace transform of (3a) and (3b) under various excitation and loading conditions. Unless otherwise stated, the 2-μm rule ($a = 2$ μm) is used for the interconnection width, and the substrate thickness and relative permittivity of $b_2 = 200$ μm and $\epsilon_2 = 12$, and those of the insulator of $b_1 = 1$ μm and $\epsilon_1 = 4$ are assumed, respectively, throughout this paper.

The calculated crosstalk amplitudes in semi-infinite interconnections are shown in Fig. 4. The number of the

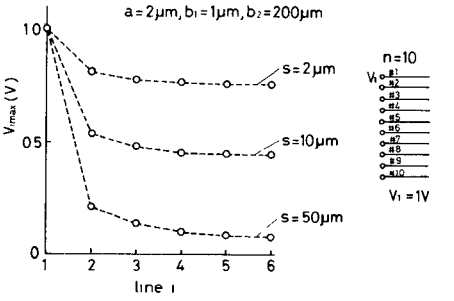


Fig. 4. Calculated crosstalk amplitude at the ith interconnection for a semi-infinite coupling length.

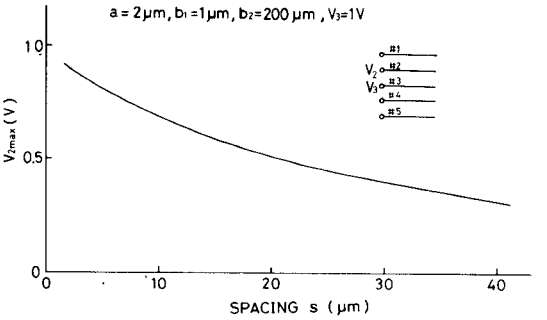


Fig. 5. Crosstalk amplitude at the adjacent interconnection for a semi-infinite coupling length plotted versus spacing s.

strips n is chosen to be ten and the input end of each strip is open circuited. A step voltage is applied to strip 1 and the induced voltage V_i at strip i is plotted versus i. This is essentially equal to the crosstalk constant as calculated from the static capacitance. It should be noted that $V_i = V_{12-i}$ because of the periodic boundary condition. Since a/b_2 is small, the shielding effect by the metallized back is small, and a voltage on one strip tends to have its effect over a long range. Fig. 5 shows the variation of induced voltage at an adjacent strip versus the spacing s ($= p - a$) calculated for $n = 5$. The long-range nature is again seen here.

C. Dynamic Excitations

In the computation of pulse waveforms on the finite-length interconnections, the input and output impedances of a logic gate are represented by a capacitor C_L and a resistor R_S. A standard 1-μm-gate GaAs MESFET with a gate width of 20 μm has approximately an input capacitance of 20 fF. The output signal impedance of a gate consisting of FET-type devices is approximately equal to the inverse of the transconductance g_m of the switching or load device which is taking part in the transient.

An example of calculated crosstalk pulse waveforms is shown in Fig. 6. The excitation and loading conditions are shown in the inset. The voltage waveform at the input of the gate terminating interconnection 4 is shown. The dashed curve shows the response calculated by the "lumped capacitance" approximation of the interconnection (explained in the Appendix) where interconnections are represented by a capacitance network shown in the inset. Clearly the "lumped capacitance" approximation becomes inadequate

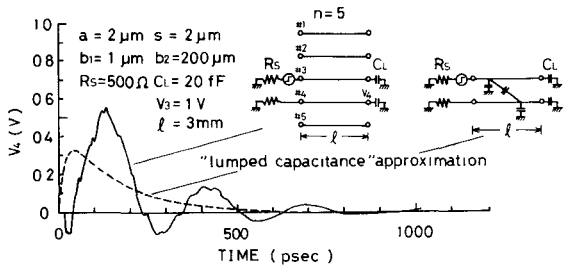


Fig. 6. Calculated step-response waveforms The dashed curve is the waveform by the "lumped capacitance" approximation.

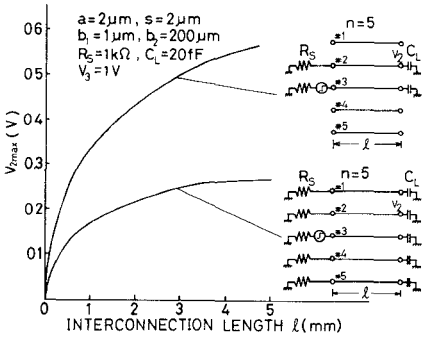
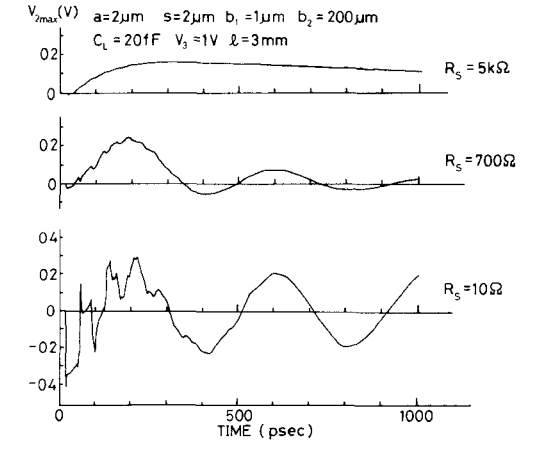
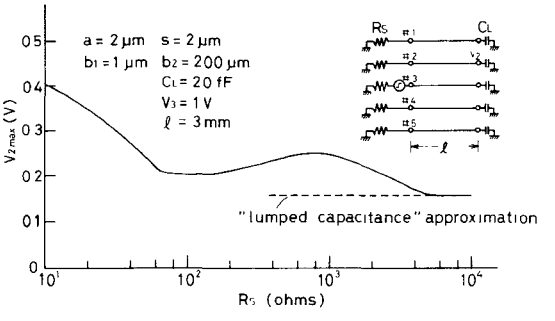


Fig. 7. Crosstalk amplitude plotted versus the interconnection length.



(a)



(b)

Fig. 8. (a) Crosstalk waveforms for different signal source resistances R_s of the gate and (b) the crosstalk amplitude plotted versus R_S.

in high-speed circuits. The results of the calculation showed that this approximation is applicable to interconnections of a few millimeters long, only when the circuit rise time is above 200–300 ps. The response waveform in Fig. 6 shows an initial time delay and a ringing-type decaying oscillation with ripple-like smaller oscillations being superposed. The initial delay is due to the propagation of wavefront, and small oscillations are due to the velocity difference of the various modes involved. On the other hand, the large amplitude oscillation with a much slower period than the round-trip times of the normal modes is due to an LC-type oscillation where the zero-mode ($\theta = 0$) with a high characteristic impedance (several kilohms) provides an effectively large lumped inductance and becomes resonant with the load capacitance.

The crosstalk amplitude is plotted versus the interconnection length in Fig. 7 for the terminal conditions shown in the inset. As seen in Fig. 7, the presence of floating interconnections has a large effect on the crosstalk amplitude because it effectively increases mutual coupling by reducing the line capacitances.

The dependences of the crosstalk waveform and amplitude on the signal source resistance R_S are shown in Fig. 8(a) and (b), respectively. The lumped capacitance approximation holds when R_s is above 2–3 kΩ and the response is slow. As the signal source resistance is reduced, the above-mentioned lumped LC oscillation becomes dominant and determines the crosstalk amplitude. With further reduction of R_s down to several tens of ohms, multiple reflection of the wavefronts of the low-impedance modes appears at the initial stage and the first negative peak of this transient determines the crosstalk amplitude. Thus, the dependence of the crosstalk amplitude on the R_s becomes complicated, as shown in Fig. 8(b), showing in the medium resistance range of 10^2–10^3 Ω a significant deviation from the general trend of increased crosstalk amplitude with the decrease of R_s.

D. Reduction of Crosstalk

From the above results, reduction of crosstalk seems imperative for successful realization of very high-speed LSI/VLSI's with sufficient noise margins to ensure reliable operation. The reason for large crosstalk is that the conventional interconnection system does not have a solid shielding ground plane in its vicinity. Therefore, one obvious way to reduce crosstalk is to reduce the substrate thickness. The effect of substrate thickness on the coupling in semi-infinite interconnections is shown in Fig. 9. It is clear that this approach is not too effective unless the substrate thickness is reduced to 10 μm, which is practically impossible unless a new technology such as SOI is employed.

Another way of reducing crosstalk is to provide adjacent shielding ground lines. A result of dynamic response calculation to investigate its effect is shown in Fig. 10 for the terminal conditions shown in the inset. Thus, it is significantly effective in reducing crosstalk. However, the computed pulse waveforms at the centers of the active line, shield line, and adjacent line, as shown in Fig. 11, exhibit dynamic ringing due to the aforementioned LC-type oscil-

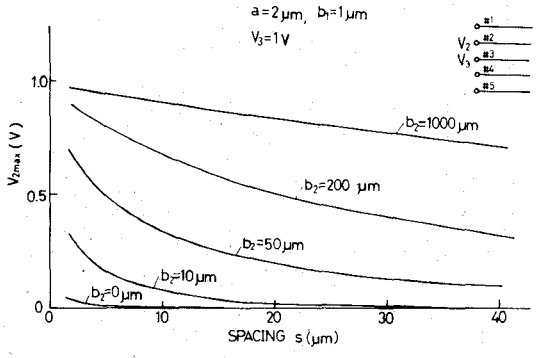


Fig. 9. Crosstalk coupling coefficient versus spacing for various substrate thickness.

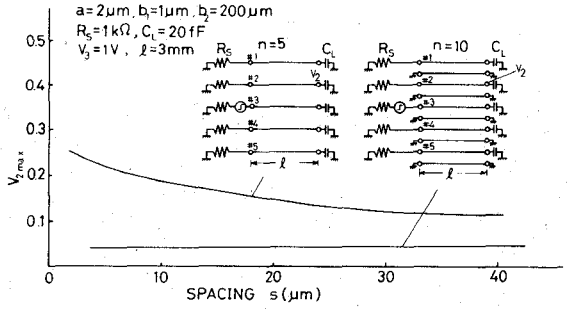


Fig. 10. The effect of shield lines on crosstalk.

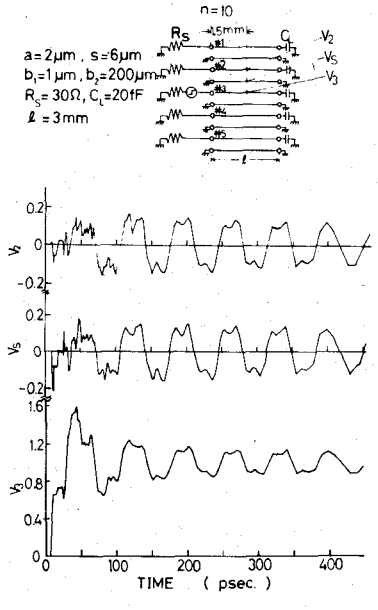


Fig. 11. Waveforms at the centers of the adjacent line (V_2), the shield line (V_S), and the active line (V_3).

lation. The potential on a narrow shield line cannot be made null all the way along the line, even if the line is grounded at both ends. Additionally, shield lines reduce the wiring channel capacity a great deal in spite of the fact that availability of interconnection capacity itself is a big problem in LSI/VLSI design.

An alternative shielded multilevel planar interconnect scheme is schematically shown in Fig. 12. The coupling in this scheme is roughly equal to the case of $b_2 = 0$ in Fig. 9 and is very small. This allows reduction of crosstalk without

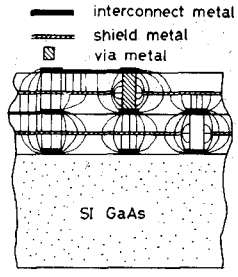


Fig. 12. A proposed shielded multilevel planar-interconnect scheme.

reducing the wiring channel capacity. The risk of dynamic ringing is reduced for a fixed value of R_s because reduction of inductance shifts the ringing frequency towards higher frequencies. Additionally, each interconnection can be regarded as a separate transmission line in this scheme, thereby facilitating the timing and layout design a great deal. On the other hand, such a scheme, of course, lowers impedance and increases capacitance. To achieve high speed and a high integration level by this scheme, devices should therefore possess high transconductance and low power consumption. Such a requirement is an essential one in any well-shielded interconnect structure, including the present one, unless the chip size is greatly reduced or the basic architecture of the integrated circuits is modified in such a way that only short interconnections are required.

IV. Conclusion

The main conclusions of the present study are as follows.

1) Crosstalk consideration is supremely important in very high-speed LSI/VLSI design with t_{pd} below a few 100 ps.

2) When the circuit speed is less than 200–300 ps in the LSI level, the "lumped capacitance" approximation for interconnection is inadequate in calculating the crosstalk waveform and amplitude, and a proper microwave consideration becomes a necessity.

3) The length, spacing, and termination conditions of interconnection, substrate thickness, and output impedance of gates have large and complicated effects on crosstalk.

4) Shield lines reduce crosstalk, but there is a risk of dynamic ringing. They also limit the wiring capacity. A shielded multilevel interconnect scheme is proposed which reduces crosstalk with reduced risk of ringing and without reduction of wiring capacity. It also facilitates timing and layout design.

Appendix
Crosstalk in the "Lumped Capacitance" Approximation

Using the circuit model shown in the inset of Fig. 13, the crosstalk amplitude $V_2(t)$ at time t is given by

$$V_2(t) = \tfrac{1}{2}(e^{-t/\tau_1} - e^{-t/\tau_2}) \qquad \text{(A1)}$$

where

$$\tau_1 = R(C + C_L) \qquad \tau_2 = R(2C_m + C + C_L). \qquad \text{(A2)}$$

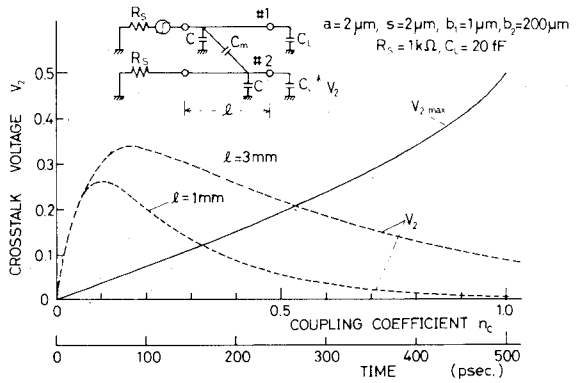


Fig. 13. Crosstalk waveform and amplitude based on the "lumped capacitance" approximation.

The maximum crosstalk amplitude is given by

$$V_{2\max} = \tfrac{1}{2}\left(e^{-(1-n_c)/(2n_c)\ln(1+n_c)/(1-n_c)} - e^{-(1+n_c)/(2n_c)\ln(1+n_c)/(1-n_c)}\right) \quad \text{(A3)}$$

where n_c is the capacitance coupling coefficient, and is given by

$$n_c = \frac{c_m}{c_m + C + C_L}. \quad \text{(A4)}$$

The crosstalk waveform and the maximum crosstalk amplitude is plotted versus time and n_c, respectively, in Fig. 13.

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